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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/817,216	03/27/2001	Yasuhiko Kuriyama	205263US2	7926

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EXAMINER

CHOE, HENRY

ART UNIT	PAPER NUMBER
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2817

DATE MAILED: 01/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary

Application No.
09/817,216

Applicant(s)
Kuriyama

Examiner
Henry Choe

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2817



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Mar 27, 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above, claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2, 6-8, 10, 12, and 16-18 is/are allowed.
- 6) ☒ Claim(s) 1, 9, and 11 is/are rejected.
- 7) ☒ Claim(s) 3-5 and 13-15 is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- a) ☒ All b) ☐ Some* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- *See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

- 15) ☒ Notice of References Cited (PTO-892) 18) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 19) ☐ Notice of Informal Patent Application (PTO-152)
- 17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 2 20) ☐ Other:

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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Maeda et al (Fig. 27).

Regarding claim 1, Maeda et al (Fig. 27) discloses a power amplifier circuit comprising a first capacitor element (2735) which is connected between a signal input terminal (2701) and an input terminal (2702) of the first transistor (2240), a second capacitor element (2736) which is connected between the signal input terminal (2701) and an input terminal (2703) of the second transistor (2244), and a first impedance element (2720) which is connected between the respective input terminals (2702 and 2703) of the first (2240) and second (2244) transistors.

Regarding claim 9, Maeda et al (Fig. 27) also discloses a power amplifier circuit comprising a bias circuit (2731, 2732, 2733, 2734) for supplying a direct current bias voltage to the respective input terminals of the first and second transistors [a bias circuit (2731 and 2732) supplies a direct current bias voltage to the input terminal (2702) of the first transistor (2240) and

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a bias circuit (2733 and 2734) supplies a direct current bias voltage to the input terminal (2703) of the second transistor (2244); see column 23, lines 43-46].

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda et al (Fig. 27).

Maeda et al (Fig. 27) further discloses a power amplifier circuit comprising a plurality of impedance elements (2732 and 2734) which are connected between the respective input terminals (2702 and 2703) of the first (2240) and second (2244) transistors and bias terminals (2731 and 2733). This arrangement is functionally equivalent to the claimed impedance elements connected between the transistor input terminals and a bias output terminal.

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Allowable Subject Matter

5. Claim 3-5 and 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Allowance

6. Claims 2, 6-8, 10, 12 and 16-18 are allowed.
7. The following is a statement of reasons for the indication of allowable subject matter: Regarding claim 2, the closest prior art of record, Shapiro et al discloses an amplifier circuit comprising a first inductor element (19) and a first capacitor element (17) connected in series between the signal input terminal (11) and an input terminal (base of transistor 15) of the first transistor (15), a second inductor element (20) and a second capacitor element (18) connected in series between the signal input terminal (11) and an input terminal (base of transistor 16) of the second transistor (16), a third inductor element (29) which is connected between an output terminal (collector of transistor 15) of the first transistor (15) and the signal output terminal (outpt), and a fourth inductor element (30) which is connected between an output terminal (collector of transistor 16) of the second transistor (16) and the signal output terminal (outpt). However, Shapiro et al does not disclose the following limitation: a first impedance element connected between the respective input terminals of the first and second transistors [It should be noted that the elements (21, 23, 24, 22) shown in the reference of Shapiro et al cannot be read as

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the first impedance element claimed in the claim 2 since the current is flowing from the inductor (21 or 22) to the ground through the resistor (23 or 24) and it (current) never flows from the inductor (21) to the inductor (22) and therefore is not "connected between the respective input terminals of the first and second transistors". Regarding claim 3, the closest prior art of record, Maeda et al (Fig. 27) does not disclose the following limitation: a second power amplifying section and a second impedance element. Regarding claim 13, the closest prior art of record, Maeda et al (Fig. 27) does not disclose the following limitation: a plurality of amplifiers connected in cascade.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patent numbers (6,201,445; 5,694,085; 5,949,287) are the parallel amplifiers with the matching circuits

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry Choe whose telephone number is (703) 305-0576.

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A handwritten signature in cursive script, appearing to read "Henry Choe".

Name: Henry Choe

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#460

January 23, 2002